Remarks

On page 3 of the Office action, paragraph 5, claims 1-4, 6, 9-10 were rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. ('154). Applicant respectfully directs the Examiner's attention to column 4, lines 40-45 of the Lee '154 patent. Lee has three embodiments consisting of "one flash memory and one mask ROM transistor, two flash transistors, and two MASK ROM transistors." On the other hand, Applicant has claimed three memory cells consisting of (1) a select transistor and a floating gate transistor (which could be a flash transistor) in Fig. 2, (2) a ROM transistor in one memory state and a select transistor in Fig. 4 and (3) a ROM transistor in the second memory state and a user programmable select transistor in Fig. 6. In each of these three cases, Applicant has a user programmable select transistor. In no case does Lee have this. In order to more clearly distinguish Applicant's invention, the user programmability and mask programmed aspects have been inserted into claim 1.

At the bottom of page 3 of the Office action, the Examiner characterizes Fig. 7D of Lee as including a select transistor. This is a gross mischaracterization of the Lee patent. In column 5, line 51 Lee states:

> "As discussed above, the conventional 2T cell contains a floating gate cell and a select transistor. However, this novel 2T cell structure M41 comprises a floating gate cell (M51a) and a 'Mask ROM' cell M41b)."

Thus, Lee eliminates the select transistor. Again, at column 6, line 20 Lee states: "The select transistor is not capable of data bit storage. Therefore, the novel 2T cell structure M41 of the present invention doubles the memory density - one-half in flash memory form, and one half in mask ROM form - without increasing area." In other words, Lee teaches that select transistors are avoided in his invention because they are not capable of storing data. Lee doubles the

memory density by using what might have been a select transistor as a memory transistor. Applicant does not do this. Applicant uses and claims a select transistor in combination with three types of memory transistors. Lee specifically teaches away from Applicant's invention by eliminating a user programmable select transistor.

The Examiner speculates that the non-volatile memory cells and read-only memory cells of Lee have the same footprint in the last line of page 3 of the Office action. There is no such teaching in Lee. The reference to column 13, lines 13-32 merely states that Lee relies on the same process for cell formation. This does not mean that both cells have the same footprint. It is quite possible, that in shorting the control gate to the floating gate with a contact 76b, as taught by Lee in column 13, lines 21-24 that there is a changed footprint. Lee shows no footprint drawings and the Examiner's remarks are speculation based upon side views, not top views from which footprints could be determined. Reliance on the "same process" as stated by Lee does not necessarily mean the same footprint.

On page 4, line 3 of the Office action the Examiner relies upon the cells "inherently" having the same footprint. The reference to "inherently" means that the reference does not specifically teach this, but the Examiner believes that the cells will have the same footprint by inherency. MPEP Section 2112 IV states that the Examiner must provide evidence tending to show inherency. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." In re Robertson, 169S3D743, 745; 49 USPQ 2d 1949, 1950-51 (CAFC 1999). In the present situation, inherency depends on the configuration of masks which are not shown in the Lee patent. The Lee patent only shows electrically operative portions of a semiconductor device, not electrically marginal portions, such as active region boundaries. Even the electrically active portions in Lee may have a lateral extent

which is not visible in the Lee patent and which is a different areawise footprint. The Examiner seems to assume that because the vertical constructions are very similar, the same areawise footprint occurs. The Examiner's position regarding inherency cannot be maintained.

It should be noted that the fourth line on page 4 the transistor 70(b) in Fig. 7B and 7D is a complete misstatement. The sentence reads: "Noted (sic) that transistor 70b in fig. 7B and 7D (column 6 line 5) can be used as select transistors." In column 6, line 5 referenced by the Examiner, Lee is stating that a select transistor is not needed because, according to Lee, "the mask ROM transistor can perform the select transistor function." Further in column 6, line 20 Lee states that "the select transistor is not capable of data bit storage." Lee's position is that select transistors are not needed and, by eliminating select transistors, he is able to double the memory density as stated in column 6, line 22.

Further on page 4 of the Office action, with regard to claim 3, the Examiner asserts that Lee discloses in column 6, line 5 a memory array with a footprint having a longitudinal dimension and a width dimension that are the same for different types of memory cells. There is no such teaching in Lee regarding footprints or any types of dimensions. The Examiner is apparently speculating that because the electronic schematics for various memory cells are the same, that the chip footprint will be the same. Such speculation is not warranted. In the middle of page 4 of the Office action, with regard to claim 4, the Examiner asserts that Lee discloses in column 13, lines 1-12 a memory array where some transistors have open channels and other cells have a shorted channel. Lee does not have the teaching stated by the Examiner. Reading lines 1 thru 12 of column 13, Lee teaches changing the threshold voltage V_{th} by varying the amount of implant. Lee does not state that open and shorted conditions are achieved, but merely that the threshold voltage is varied. The same is true with the

Examiner's language with regard to claim 9 at the bottom of page 4 of the Office action. There is no teaching about "the extent of the implant defining open and shorted channels" as stated by the Examiner. The Examiner is reading Applicant's claim limitations into the teachings of Lee which is an improper technique in patent examination.

At the top of page 5 of the Office action, the Examiner asserts that Lee teaches a memory array with EEPROM transistors. There is no teaching of an EEPROM transistor in combination with the user programmable select transistor.

On page 5 of the Office action, claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. Claims 7 and 8 ultimately depend upon claim 1 wherein each cell includes a user programmable select transistor. As described above, Lee teaches away from use of select transistors in memory cells. Claims 7 and 8 have been rejected improperly because a person following the teachings of Lee would be led away from use of select transistors in combination with the read-only memory cells in the attempt according to Lee, to achieve double density.

On page 6 of the Office action, claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '154 in view of Hsu et al. ('286). Claim 5 is dependent on claim 1 and therefore includes the limitations thereof discussed above. The combination of Hsu and Lee cannot cure the defect of Lee teaching away from Applicant's invention. The Examiner maintains that Lee, in Fig. 7B, "has two poly layers", paragraph 8 of the Office action, line 4. It could be contended that Lee has three poly layers, not two, with the third poly layer being contact 76b. Lee does not specifically teach a material of contact 76(b). However, if Applicant is allowed to make the same "inherency" argument that the Examiner has made, the contact 76b is inherently poly since poly is used for the other conductive layers and Lee speaks of using "the same process" column 13, line 17 in modifying a flash cell to

become a ROM cell. Accordingly, if Lee has three poly layers, there is an additional reason that the rejection of claim 5 must fail.

Reconsideration is requested in view of the amendment and remarks herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

Thomas Schneck

Thomas Schneck
Reg. No. 24,518
Schneck & Schneck
P.O. Box 2-E
San Jose, CA 95109-0005
(408) 297-9733

CERTIFICATE OF TRANSMISSION
UNDER 37 CFR §1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with §1.6(a)(4) on the date shown below.

Signed: Merle P. Garcia
Typed Name: Merle P. Garcia

Date: April 9, 2007